Job Title: Internal Research Fellow (Postdoc) in On-Board Data Processing

Req ID **2204** - Posted **20/09/2017**

EUROPEAN SPACE AGENCY

Research Fellow opportunity in the Directorate of Technology, Engineering and Quality.

ESA is an equal opportunity employer, committed to achieving diversity within the workforce and creating an inclusive working environment. Applications from women are encouraged.

Post

Internal Research Fellow (Postdoc) in On-Board Data Processing
This post is classified F2 on the Coordinated Organisations' salary scale.

Location

ESTEC, Noordwijk, The Netherlands

Description

On-board payload data processing work is based in the On-Board Payload Data Processing Section in the Data Systems and Microelectronics Division at ESTEC. Our competences include:

- Data processor architectures
- Data acquisition chains
- High speed on-board networks
- Digital signal processing, processors and specialised devices
- Payload data storage
- Image and signal processing algorithms
- Data compression techniques
- High rate data encryption

As part of ESA's Directorate of Technical and Quality Management, the Section provides technical support in its domain of competence to all programme directorates in order to support their missions and developments. The Section is also responsible for initiation and execution of technology developments that may lay the foundation for future missions. This comprises developments in analogue and digital hardware from components to subsystems and building blocks, low-level software and novel signal processing techniques.

In particular, the Section hosts the centre of expertise for data compression algorithms, techniques and devices. It has initiated the development and standardisation of SpaceWire and SpaceFibre links, nodes and networks which have become very widely used not only in nearly all European space missions but also in the US, Japan, Russia and around the world.

Interested candidates are encouraged to visit the ESA website for more information regarding the Division's activities.

Field(s) of activities/research

This research fellow position provides an opportunity for interested researchers to enhance the understanding of how reconfigurable space-qualified and COTS FPGAs, such as Microsemi RTG4 (flash-based), Xilinx Virtex/ Zynq and ESA's BRAVE (SRAM-based), can be implemented in current and future on- board data processing units in an efficient way. While the fault tolerance of such devices is a rich research topic on its own, the research will be focused on how these devices are best used from a system engineering perspective, including:

- The upload of full bitstreams to the spacecraft and the (partial) patching of bitstreams, including an investigation of possible compression schemes for interplanetary missions with low-speed upload data rates;

- The storage of bitstreams in memory, including an analysis of the optimal location and the required mechanisms e.g. to load the bitstream from a mass memory unit to the working memory of the payload instrument, to verify the correctness of the transfer and to execute scrubbing of the memory, if required;
- The full and (depending on the device technology) partial configuration of the FPGA depending on mission phases or processing tasks to be performed. This crucial step requires special attention to ensure that neither the device itself nor any attached device is harmed due to a faulty configuration. An analysis should show up potential risks (e.g. accidentally reprogrammed Input/Output blocks) and suggest fault isolation schemes on unit level;
- Even if it is known that the bitstream is downloaded correctly to the FPGA device, it would be interesting to execute some basic hardware validation before operation. For instance, the implemented hardware could be tested in flight, by stimulating it with test vectors on its inputs and by comparing its outputs to a known signature. It could be researched how to store and compress the vectors efficiently and how to write and read them to/from the device (JTAG boundary scan, NAND tree etc.);
- A boot loader concept that implements – similar to a software boot loader – TM/TC functionality to execute the abovementioned steps (upload, download, de-compression, memory copy, memory verification, full and partial reconfiguration of the FPGA, verification of correct functionality of the FPGA). The boot loader should also take into account: (i) systems with multiple FPGAs, and (ii) systems that use the FPGAs as accelerators i.e. that want to dynamically request the installation of new hardware blocks from a main software running on a microprocessor. A trade-off study could reveal the pros and cons of implementing this boot loader (i) external to the instrument, e.g. within the on-board computer, (ii) within the instrument in a dedicated microprocessor and (iii) even within the FPGA itself in either a hard or soft microprocessor.

Technical competencies

Ability to conduct research autonomously
Breadth of exposure coming from past and/or current research/activities
Research/publication record
Knowledge relevant to the field of research
Interest in space and space research
Ability to gather and share relevant information

Behavioural competencies

Innovation & Creativity
Continuous Learning
Self Motivation
Communication
Problem Solving
Relationship Management
Cross-Cultural Sensitivity

Education

Applicants should have recently completed, or be close to completion of a PhD in electrical engineering, preferably with a background in Field Programmable Gate Arrays (FPGAs). Preference will be given to applications submitted by candidates within five years of receiving their PhD.

Additional requirements

The working languages of the Agency are English and French. A good knowledge of one of these is required. Knowledge of another Member State language would be an asset.

Other information

For behavioural competencies expected from ESA staff in general, please refer to the ESA Competency Framework.

The Agency may require applicants to undergo selection tests.

The closing date for applications is 18 October 2017.

In addition to your CV and your motivation letter, please add your proposal of no more than 5 pages outlining your proposed research. Candidates must also arrange for up to three letters of reference to be sent by e-mail, before the deadline, to temp.htr@esa.int. The letters must be sent by the referees themselves. The candidate's name must be mentioned in the subject of the email.

If you require support with your application due to a disability, please email contact.human.resources@esa.int.

Please note that applications are only considered from nationals of one of the following States: Austria, Belgium, the Czech Republic, Denmark, Estonia, Finland, France, Germany, Greece, Hungary, Ireland, Italy, Luxembourg, the Netherlands, Norway, Poland, Portugal, Romania, Spain, Sweden, Switzerland, the United Kingdom and Canada and Slovenia as well as Bulgaria, Cyprus, Latvia, Lithuania, Slovakia as European Cooperating States (ECS).

Priority will first be given to candidates from under-represented Member States.

In accordance with the European Space Agency's security procedures and as part of the selection process, successful candidates will be required to undergo basic screening before appointment