Research Fellowship in Microcontrollers

Directorate of Technical and management Support

ESTEC, Noordwijk, The Netherlands

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Overview of the Division's mission

The Data Systems Division is responsible for project support and technology development of space applications for all that concerns on-board data handling and processing systems (essentially control computers, data handling computers, specialised processors for payload data processing, solid state mass memories, microelectronics devices, ASICs, command and control busses, on board networks and corresponding support software).
The division is, besides activities related to the specification and validation of data systems, also actively involved in the design of the required building blocks. These elements must comply with high reliability and availability requirements combined to specific immunity to the space environment, in particular related to radiation induced effects.
The division hosts several laboratory facilities (for Avionics and Payload Data systems) that allow hands-on work.

Overview of the field of research proposed

Background

New space-grade distributed intelligence control units are subject to requirements regarding safety, availability and reliability. This is due to new functionalities (autonomous loop control, digital interface management) on the one hand and the growing cross-linking of different functionalities on the other hand. When designing systems of this kind it is required to choose an appropriate combination of hardware and software components. These must fulfill the functional requirements as well as safety requirements and must not violate any other non-functional requirements such as budgets and energy consumption.

Task

The task in this research work will start from the examination of requirements developing reference use case applications. The Research Fellow may on the one hand compare different applications with each other (e.g. active thermal control vs. motor control vs. interface management), or on the other hand examine what kind of requirements result from implementing multiple conditionally safety-critical and non-safety-critical applications on a single controller. The Research Fellow will consider the Space Avionics Open Interface aRchitecture (SAVOIR) that is an high level avionics architecture defined by the agency in collaboration with national agencies , Primes and Equipment suppliers that covers the current and near future needs for Science, Earth Observation and Telecom missions.

A critical study of commercial (mainly automotive) standards in this field and their applicability to space designs could be necessary. These are:
IEC 61508
ISO 26262
IEC 60730 and IEC 60335
EN ISO 13849

These newer standards recognize the need for protection against both random and systematic failures in terrestrial safety critical systems. Random failures are usually component failures either intrinsic or generated by space radiation effects, and are related to reliability and FIT numbers. Systematic failures are usually software and hardware design method failures. To put it simply, these failures are caused by an imperfect design.

The primary method used to mitigate failures of both types is with self-testing. Some processor features that assist in designs targeting these standards include the CPU self-test block, a replicated, safety enhanced watch-dog timer, memory ECCs on peripheral/DMA/interrupt memories, parity or CRC checks on all communication channels, memory built-in self-test (BIST), clock and supply voltage monitoring, on-chip clock or dual clocks, a junction temperature sensor, and dual A/Ds with shared channels.

Design, test and implementation of new or existing robust architectures for space grade (micro) controllers will be the main target of this RF. Possible update(s) of the SAVOIR architecture will be an additional output.

Having safety handled with hardware (the processor) instead of code can speed up development, provide transparent (in SW terms) error detection, improve safety, and ease space system's qualification efforts.
There are also a few automatic code generators in this area to consider and perhaps an IDE employing model-based development. Of course the OS, if you have one, needs to be safety aware, and a quality C/C++ compiler, for a higher abstraction level and support for object-oriented programming, will be essential.

The Research Fellow will join a young, dynamic, multi-national team.

Who can apply

The programme is open to suitably qualified women and men. Preference will be given to applications submitted by candidates within five years of receiving their PhD.

The Research Fellow Programme is open to nationals of the following states: Austria, Belgium, the Czech Republic, Denmark, Finland, France, Germany, Greece, Ireland, Italy, Luxembourg, the Netherlands, Norway, Poland, Portugal, Romania, Spain, Sweden, Switzerland, and the UK, or Canada as a Cooperating State, Bulgaria, Estonia, Hungary, Latvia, Slovakia and Slovenia as European Cooperating States (ECS).

Required qualifications

Applicants must have recently completed their PhD studies in Physics, Electrical engineering or comparable.
Expertise in computer science, digital design (VHDL, Verilog) and Embedded SW is required.

Applicants should have good analytical and communication skills and should be able to work in a multi-cultural environment in an autonomous manner.

Applicants must be fluent in English and/or French, the working languages of the Agency. A good proficiency in English is required.

How to Apply

Please fill in the online application form attaching to it, **in one document only,** your CV, your motivation letter and your research proposal.

Candidates must also arrange for up to **three letters of reference** to be sent by e-mail, before the deadline, to **temp.htr@esa.int**. The letters must be sent by the referees themselves. The candidate's name must be mentioned in the subject of the email.

Applications satisfying the general conditions for eligibility, to be submitted **by 6 May 2015**, will be evaluated and successful applicants will be invited for an interview.

Interested candidates are highly encouraged to visit the ESA website: www.esa.int.